Homework 12

Problem 1

The following table gives the parameters for a number of different caches. Fill in the missing fields in the table for each cache. Recall that **m** is the number of physical address bits, **C** is the cache size (number of data bytes), **B** is the block size in bytes, **E** is the associativity, **S** is the number of cache sets, **t** is the number of tag bits, **s** is the number of set index bits, and **b** is the number of block offset bits.

Cache	m	C	B	E	S	t	s	b
1	32	1024	4	4				
2	32	1024	4	256				
3	32	1024	8	1				
4	32	1024	8	128				
5	32	1024	32	1				
6	32	1024	32	4				

Problem 2

The following table gives the parameters for a number of different caches. Fill in the missing fields in the table for each cache. Recall that **m** is the number of physical address bits, **C** is the cache size (number of data bytes), **B** is the block size in bytes, **E** is the associativity, **S** is the number of cache sets, **t** is the number of tag bits, **s** is the number of set index bits, and **b** is the number of block offset bits.

Cache	m	C	B	E	S	t	s	b
1	32		8	1		21	8	3
2	32	2048			128	23	7	2
3	32	1024	2	8	64			1
4	32	1024		2	16	23	4	

Problem 3

Suppose we have a system with the following properties:

1) The memory is byte addressable.
2) Memory accesses are to 1-byte words (not to 4-byte words).
3) Addresses are 12 bits wide.

The cache is **two-way set associative** (E=2), with a **4-byte block size** (B =4) and **four sets** (S =4). The contents of the cache are as follows, with all addresses, tags, and values given in hexadecimal notation:

Set Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	00	1	40	41	42	43
	83	1	FE	97	CC	D0
1	00	1	44	45	46	47
	83	0	--	--	--	--
2	00	1	48	49	4A	4B
	40	0	--	--	--	--
3	FF	1	9A	C0	03	FF
	00	0	--	--	--	--

A. The following diagram shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

CO **The cache block offset**

CI **The cache set index**

CT **The cache tag**

11	10	9	8	7	6	5	4	3	2	1	0

B. For each of the following memory accesses, indicate if it will be a cache hit or miss when carried out **in sequence** as listed. Also give the value of a read if it can be inferred from the information in the cache.

Operation	Address	Hit (Y or N)	Read value (or unknown)
Read	0x834		
Write	0x836		--
Read	0xFFD		