ICS13' Homework 2 Solution

1. SEQ:

	Generic	Specific
Stage	Call Dest	Call 0x029
Fetch	icode:ifun←M1[PC] valC←M4[PC+1] valP←PC+5	icode:ifun←M1[0x023]=8:0 valC←M4[0x024]=0x029 valP←0x023+5=0x028
Decode	valB←R[%esp]	valB←R[%esp]=128
Execute	valE←valB+(–4)	valE←128+–4=124
Memory	M4[valE]←valP	M4[124]←0x028
Write Back	R[%esp]←valE	R[%esp]←124
PC update	PC←valC	PC←0x029

2. PIPE Basic:
   SEQ: 6hours
   PIPE:3.5hours
   SpeedUp: 6/3.5 = 1.71

3. Hazard Basic:
   Data Hazard:
   Instruction depends on result of prior instruction still in the pipeline

   Control Hazard:
   Caused by delay between the fetching of instructions and decisions about changes in control flow

4. Data Hazard:
   There is a load/use hazards between mrmovl(2) and mrmovl(3) and a load/use hazards between mrmovl(3) and addl(4). Data hazard between addl(1) and mrmol(2) can be solved by forwarding.

5. Forwarding:
   1) In cycle 4, the decodestage logic detects a pending write to register%edxin the memory stage. It also detects that a new value is being computed for register%eaxin the execute stage. It uses these as the values for valA and valB rather than the values read from the register file
   2) No, in this Five Stages Pipelining, Read in Stage 2, Write in Stage 5.

6. Open Question:
   Anything you like.