Problem 1: Address Translation

In the following three problems, you are to show how the example memory system in Section 9.6.4 translates a virtual address into a physical address and accesses the cache. For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs. If there is a cache miss, enter “-” for “Cache Byte returned.” If there is a page fault, enter “-” for “PPN” and leave parts C and D blank.

(1) 0x027c (2) 0x03a9 (3) 0x0040

A. Virtual address format:

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address Translation:

VPN	TLB index	TLB tag	TLB hit? (Y/N)	Page fault? (Y/N)	PPN

C. Physical address format:

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference:

Byte offset	Cache index	Cache tag	Cache hit? (Y/N)	Cache byte returned

Problem 2: Multi-Level Page Tables

The computer has a 64-bit virtual address space and the page size is 2048B. The page table entry's length is 4B. For all pages must be included in a table, the multi-level page table is used. How many levels are needed? Please write the process of problem-solving.