# Homework 13

## Problem 1

Considering the instructions *leave* and *iaddl* in homework 4.47 and 4.48, modify the HCL descriptions of the control logic blocks to implement the two instruction. Since you have already completed some in last exercise class, so you only need to implement these logic blocks this time:
{need_valC, srcB, dstM, aluB, mem_data}

## Problem 2

Ann, Brian, Cathy, Dave each have one load of clothes to wash, dry, and fold. The machine washer takes 40 minutes, dryer takes 50 minutes, and folder takes 30 minutes to deal with one load of clothes. If they worked sequentially, how long would the whole process take? What if they used Pipelining? Please indicate the Speedup (old/new).

## Problem 3

In PIPE Implementation, how many kinds of Hazards are there? And what are the causes?

## Problem 4

Considering the codes below and answer the following questions:

| **Prog1** | **Prog2** |
|---|---|
| irmovl $1,%ebx<br>irmovl $2,%ecx<br>addl %ebx,%ecx<br>halt | rrmovl %eax,%ebx<br>rrmovl %edx,%eax |

1) How to solve above data hazard in Prog1 by Forwarding ? You can draw a picture to illustrate yourself.
2) In Prog2, Is there a *Data Hazard*? If yes, how to solve it. If no, explain why.