Homework 14 Solution

Problem 1

A pipeline stall is when a pipeline stage's input memory remains the same from one cycle to the next. A pipeline bubble is when a pipeline stage's input memory changes to that of a nop instruction, i.e., an instruction that does nothing. On any cycle when an instruction stalls in one stage, a bubble is injected into the subsequent stage.

Problem 2

If the two cases were reversed, then the write back from M_valE would take priority, causing the incremented stack pointer to be passed as the argument to the rrmovl instruction. This would not be consistent with the convention for handling popl %esp determined in section 4.1.6 in ICS book.

Problem 3

Instruction	Cause	Stage
halt	Halt	F
.byte FE	Invalid instruction	F
jmp $-100	Invalid instruction	F
rmmovl %eax,0x10000(%eax) where %eax=$100	Bad address	M
xor %eax, %eax jne t ret t: .byte 0xFF	--	--

Problem 4

CPI=1+0.15*0.2*1+0.35*0.4*2+0.01*3=1.34