Homework 11

Problem 1. In the following two problems, you are show how the example memory system in Section 9.6.4 translates a virtual address into a physical address and access the cache. For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs. If there is a cache miss, enter "-" for "Cache Byte returned." If there is a page fault, enter "-" for "PPN" and leave parts B and C blank.

1)Virtual address: 0x027c

A. Address translation

Parameter	value
VPN	0x____[1]____
TLB Index	0x____[2]____
TLB Tag	0x____[3]____
TLB Hit? (Y/N)	____[4]____
Page Fault? (Y/N)	____[5]____
PPN	0x____[6]____

B. Physical address 0x__[7]__

C. Physical memory reference

Parameter	value
Byte offset	0x____[8]____
Cache Index	0x____[9]____
Cache Tag	0x____[10]____
Cache Hit? (Y/N)	____[11]____
Cache byte returned	0x____[12]____

2)Virtual address: 0x0040

A. Address translation

Parameter	value
VPN	0x____[1]____
TLB Index	0x____[2]____
TLB Tag	0x____[3]____
TLB Hit? (Y/N)	____[4]____
Page Fault? (Y/N)	____[5]____
PPN	0x____[6]____

B. Physical address 0x__[7]__

C. Physical memory reference

Parameter	value
Byte offset	0x____[8]____
Cache Index	0x____[9]____
Cache Tag	0x____[10]____
Cache Hit? (Y/N)	____[11]____
Cache byte returned	0x____[12]____

Problem 2. The following problem concerns virtual memory and the way virtual addresses are translated into physical addresses. Below are the specifications of the system on which the translation occurs.

- Memory is byte addressable and memory accesses are to 4-byte words.
- The system is configured with 256MB of virtual memory.
- The system has only 64MB of physical memory.
- The page size is 4KB.
- The TLB is 2-way set associative with 8 total sets.

The contents of the TLB and the relevant sections of the page tables are shown below. In the following tables, all numbers are given in hexadecimal.

TLB			
Index	Tag	PPN	Valid
0	0003	03EB	1
	1A10	0D46	0
1	0107	0AD3	1
	1D01	052F	0
2	0106	0D4E	1
	1213	01D3	0
3	0301	005C	0
	0A0B	0231	1
4	1211	0819	1
	0108	03D8	0
5	011F	0218	1
	1102	0A4A	1
6	1FE7	0263	1
	103F	0FAF	0
7	0211	030D	0
	10D2	0310	0

Page Table		
VPN	PPN	Valid
0837	1457	0
0838	0D31	0
0839	0AD3	1
0840	035A	1
0841	16F3	0
0842	0D4E	1
0843	031D	1
0844	078F	1
0845	0487	1
0846	0819	0
0847	136B	1
0848	04BA	1
0849	0D33	0
0850	0061	0
0851	0328	0
0852	0F42	0

Please step through the following address translation. You may indicate a page fault by entering a '–' for Physical Page Number and Physical Address.

Parameter	value
Virtual Address	0x839108
TLB Index	0x____[2]____
TLB Tag	0x____[3]____
TLB Hit? (Y/N)	____[4]____
PPN	____[5]____
Physical Address	0x____[6]____

Problem 3. Determine the number of page table entries (PTEs) that are needed for the following combinations of virtual address size (n-bit) and page size (P):

n	P=2^p	#PTE
16	2K	
16	4K	
32	4K	
32	8K	