Homework 3 Sol

Problem 1

The following table gives the parameters for a number of different caches. Fill in the missing fields in the table for each caches. Recall that **m** is the number of physical address bits, **C** is the cache size (number of data bytes). **B** is the block size in bytes, **E** is the associativity, **S** is the number of cache sets, **t** is the number of tag bits, **s** is the number of set index bits, and **b** is the number of block offset bits.

Cache	m	C	B	E	S	t	s	b
1	32	1024	4	4	64	24	6	2
2	32	2048	4	4	128	23	7	2
3	32	1024	2	8	64	25	6	1
4	32	1024	8	128	1	29	0	3
5	32	1024	32	2	16	23	4	5
6	32	1024	32	4	8	24	3	5

Problem 2

1.
[1] 2048 [2] 23 [3] 4 [4] 5
2.
[1] 11 [2] Y [3] 11 [4] N
[5] 10 [6] Y [7] 11 [8] Y
[9] 10 [10] Y [11] 10 [12] N
[13] 66.67% (2/3)
3.
1) (1+8+8) * 3 = 51
2) [(1 + 1) + 1 + 1] / 51 = 7.84% (4/51)
3) Scheme B
Reason: The four rows of the array are in set 8, 9, 10, 11 respectively, so increasing the number of sets is useless. After doubling the block size, the miss rate is (1 + 1) / 51 = 3.92%. Each row of the array only occupies one cache line in a set, so increasing the number of ways is useless.