Solution 4

Problem 1

For each of the instruction that will cause exception, specify its cause(halt, bad address or invalid) and the stage(Decode,Fetch,Execute...) where exception can be detected, otherwise leave blank. (%eax = $100)

Instruction	Cause	Stage
halt	Halt	F
.byte FF	Invalid instruction	F
jmp $-1	Invalid instruction	F
rmmovl %eax,0x10000(%eax)	Bad address	M
xor %eax,%eax jne t t: .byte 0xFF	-	-

Problem 2

Consider we have a machine with two cache L1 cache and L2 cache
L1 cache hit time: 2 cycles
L1 cache hit rate: 95%
L2 cache hit time:10 cycles
L2 cache hit rate: 98%
Memory read time:200 cycles

The Miss Penalty of L1 cache is 10*0.98+200*0.02 = 13.8 (3.8 is also right)
The average access time is 2*0.95 + 13.8*0,05 = 2.59

Problem 3:

Consider a 12 – bit machine with a 2-way set associative cache, memory access are to 1-byte words, the contents of the cache are as follows, with Hex notation.

Set	Tag	Valid	Byte0	Byte1	Byte2	Byte3	Tag	Valid	Byte0	Byte1	Byte2	Byte3
0	0x09	1	0x86	0x30	0x3F	0x10	0x00	0	--	--	--	--
1	0x45	1	0xAB	0xCD	0xEF	0x00	0x38	0	0x00	0xBC	0x0B	0x37
2	0xEB	0	--	--	--	--	0x0B	0	--	--	--	--
3	0x06	0	--	--	--	--	0x32	1	0x12	0x08	0x7B	0xAD

1.Please fill the following blanks

[1] 32 [2] 8 [3] 2 [4] 2

2.With above cache contents, cache replacement policy is LRU, we have several sequentially executed memory accesses, please fill in the following blanks. (12’)
(NOTE: if unknown fill in ‘--’)

[1] 1 [2] Yes [3] Oxcd
[4] 1 [5] No [6] --
[7] 1 [8] Yes [9] --
[10] 1 [11] No [12] --