# Homework 2

## Problem 1

The following table gives the parameters for a number of different caches. Fill in the missing fields in the table for each cache. Recall that **m** is the number of memory address bits, **C** is the cache size (number of data bytes), **B** is the block size in bytes, **E** is the associativity, **S** is the number of cache sets, **t** is the number of tag bits, **s** is the number of set index bits, and **b** is the number of block offset bits.

| Cache | m | C | B | E | S | t | s | b |
|---|---|---|---|---|---|---|---|---|
| 1 | 64 | 4096 | 8 | 2 | 256 | 53 | 8 | 3 |
| 2 | 64 | 2048 | 16 | 4 | 32 | 55 | 5 | 4 |
| 3 | 64 | 8192 | 4 | 8 | 128 | 55 | 7 | 2 |
| 4 | 64 | 2048 | 4 | 32 | 16 | 58 | 4 | 2 |

## Problem 2

1) 16 * 16 = 256

2) 16 times, one cache miss on each iteration of the outer loop.

3) 4 * 15/16 + (200 + 4) * 1/16 = 16.5

4) Only C will reduce the miss rate into half

## Problem 3

| Operation | Address | Hit (Y or N) | Read value (or unknown) |
|---|---|---|---|
| Read | 0x3615 | Y | 0x97 |
| Read | 0x2816 | N | unknown |
| Read | 0x084F | Y | 0x9F |
| Read | 0x412b | N | unknown |
| Read | 0x5637 | N | unknown |