ICS Homework 2 Solution

March 3, 2021

1 Organization

1.1 Y86-64 Instructions

Please write down the byte codes of the following Y86-64 instructions.

Y86-64 instructions	**Byte codes (hex value)**
`rrmovq %rbx, %rdx`	0x2032
`jmp 0xabc`	0x70bc0a000000000000
`addq %rbx, %rax`	0x6030
`call 0x1234`	0x803412000000000000
`rmmovl %rcx, 0x12(%rbx)`	0x40131200000000000000
`jle 0x280`	0x718002000000000000
`pushq %rax`	0xa00f

1.2 SEQ Processor

Suppose we are going to implement **crmmovl rA, D(rB)**, which conditionally write rA to memory, in our SEQ Y86_64 processor.

1. How long is the `crmmovl` instruction? 10 bytes.
2. Fill the table below.

Stage	`crmmovl rA, D(rB)`

Fetch	`icode:ifun <- M1[PC]`
	`rA:rB <- M1[PC + 1]`
	`valC <- M8[PC + 2]`
	`valP <- PC + 10`

Decode	`valA <- R[rA]` `valB <- R[rB]`
Execute	`Cnd <- Cond(CC,ifun)` `valE <- valB + valC`
Memory	`Cnd ?  M8[valE] <- valA : -`
Write back	
PC update	`PC <- valP`

2 System Software

2.1 User & Kernel Mode

```
1  int array[10];
2  void func1(void) {
3      array[5000] = 40;
4      return 0;
5  }
6
7  void func2(void) {
8      array[5] = 40;
9      return 0;
10 }
```

During the execution of the two functions given above, will the control flow changes from user mode to kernel mode?

Executing func1 will definitely trap to kernel mode, as a page fault occurs in an invalid address.

Executing func2 may trap to kernel mode. If the array hasn't been touched before, a page fault will occur. Interrupts may also happen during its execution.

2.2 Concurrency

In table below, control flow for a series of processes is shown. A cell with * means the process is executed at current time. Among these processes, which pairs run concurrently and which pairs are sequential? (Suppose all processes finish executing at the end of time.)

Time	A	B	C	D
0	*			
1			*	
2				*
3	*			
4			*	
5		*		
6	*			

Concurrent: A&B A&C A&D C&D
Sequantial: B&C B&D